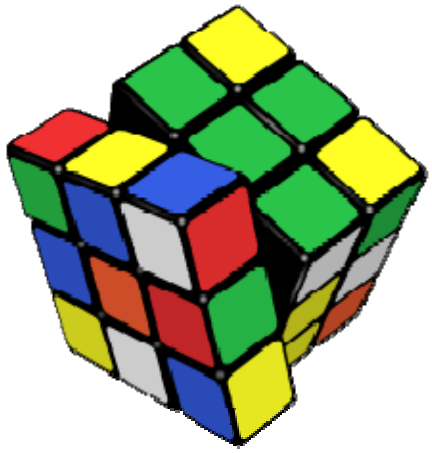

System-on-Chip Architecture for Mobile Applications

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Agenda

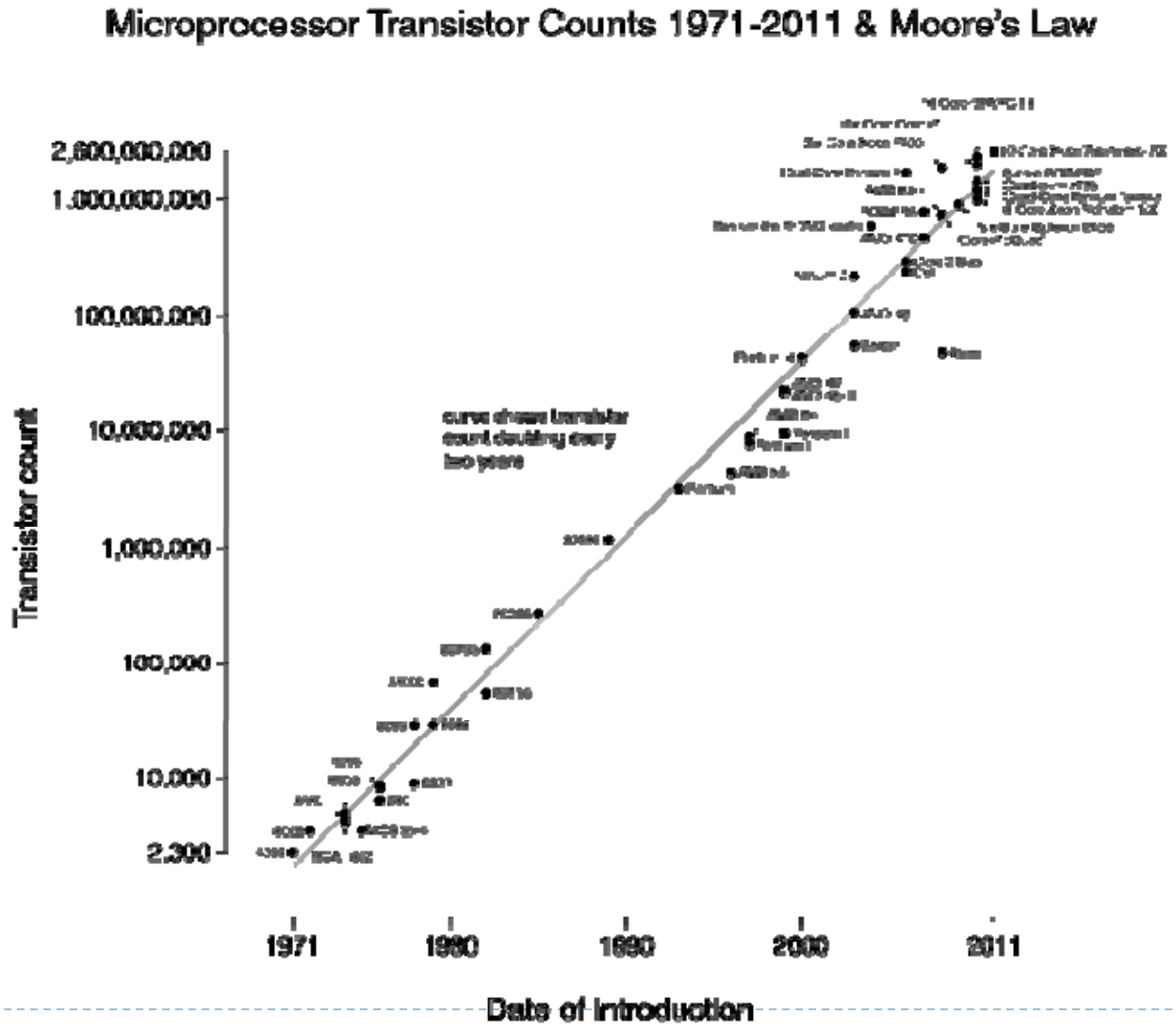
- What is Mobile Application Platform
- Challenges
- Key Architecture Focus Areas
- Conclusion

Mobile Revolution

- Commonly ARM-based single-, dual-, and quad-core CPUs for high performance mobile computing
- Multi-mode wireless modem (not in App Processors)
- Support for Wi-Fi® and Bluetooth® connectivity
- High-performance GPUs for powerful multimedia capabilities
- Integrated high accuracy GPS engine
- High-resolution display support including HDMI
- High-quality, high-resolution still image and HD up to 1080p video capture / playback
- Support for multiple mobile operating systems such as Android, Windows Phone 7, Chrome, etc.

Google | android | SAMSUNG | MOTOROLA | Sony Ericsson | htc | LG

Billion Transitor SOC

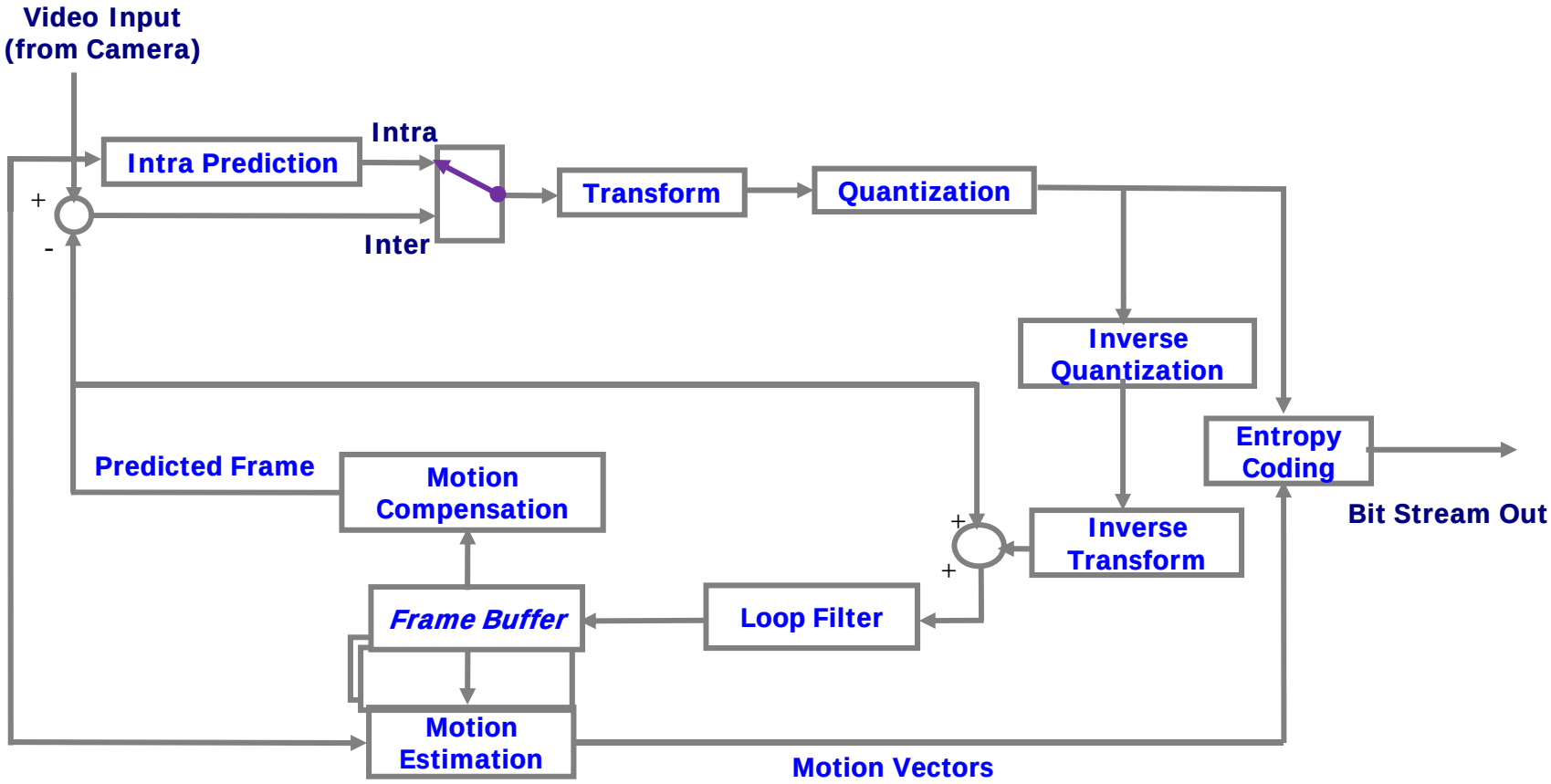


Source: http://en.wikipedia.org/wiki/Moore's_law

Trend & Challenges

- Time to market
  - Concept-to-TO
  - Faster Productization
  - Ability to change spec late in cycle
- Higher Performance
  - Higher data rate
  - Rich multimedia
  - Convergence
- Higher Integration
  - Moore's law
  - IP reuse, more features
  - Smaller technology nodes, more transistors per mm^2
- Lower Power Consumption
  - Higher battery life
  - Better Form Factor
  - Uncompromised performance
- Faster Software Boot
  - Multiple HLOS
  - Silicon to CS within 4-6 months

H.264 Encoder Block Diagram



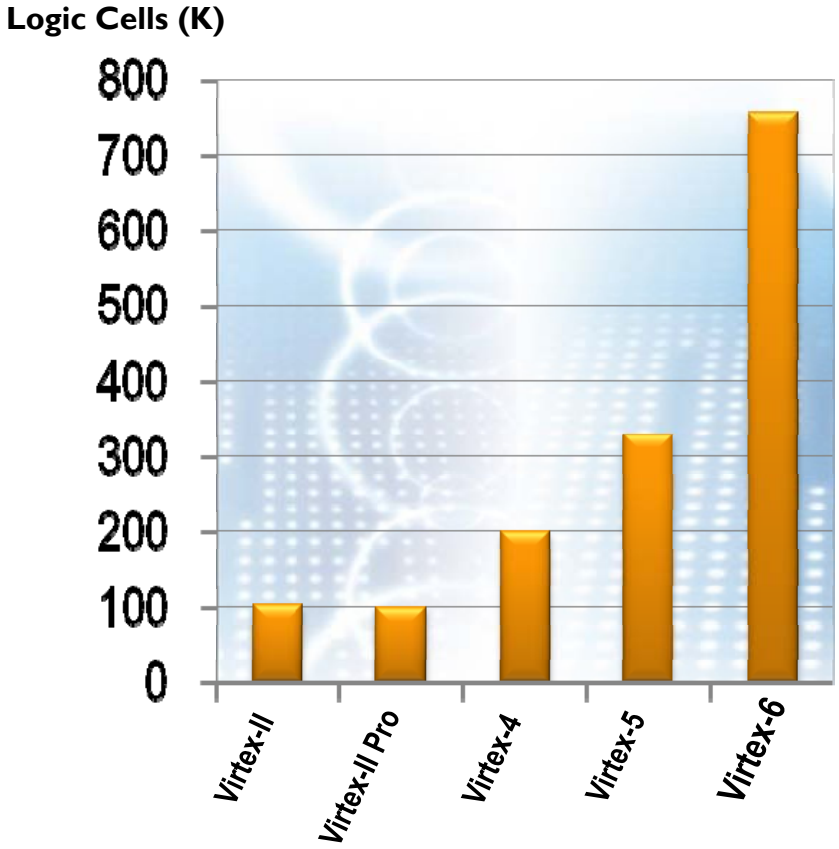
Such High Computing Requirement demands dedicated HW elements
(known as Co-processors or HW accelerators)

System-on-Chip Architecture

- Multi-core design
  - Distributed per sub-system vs. tightly coupled within a processor sub-system
  - Parallel computing and better DVFS capabilities
- High Performance System Fabric
  - Hierarchical & Reconfigurable
  - Offers access priority through tier-ed arbitration algorithms,
  - Provides protection based on master/slave transaction requirements
  - Concurrency
- Modular Sub-system Design Approach
  - Again, higher level of concurrency
  - Separate clock & power domain
  - Modular SW architecture
  - Better power and performance management
- Pre-Silicon Development & Validation
  - FPGA based ASIC prototype, Functional & Cycle-accurate SW Models
- Architecture Evolution & Reuse
  - Easier SW migration and adaptation
  - Lower development time and validation complexity

ASIC Prototyping … (1)

- ASIC prototyping is integral part of Pre-silicon validation & development.
  - SOC architect wants to do ***what-if*** analysis
  - ASIC designers want to validate their design as per spec.
  - SW engineers want to develop as much software as possible before tape-out including HLOS (Android) boot
- Higher performance achieved at lower power consumption enabling near real-time prototyping for critical blocks



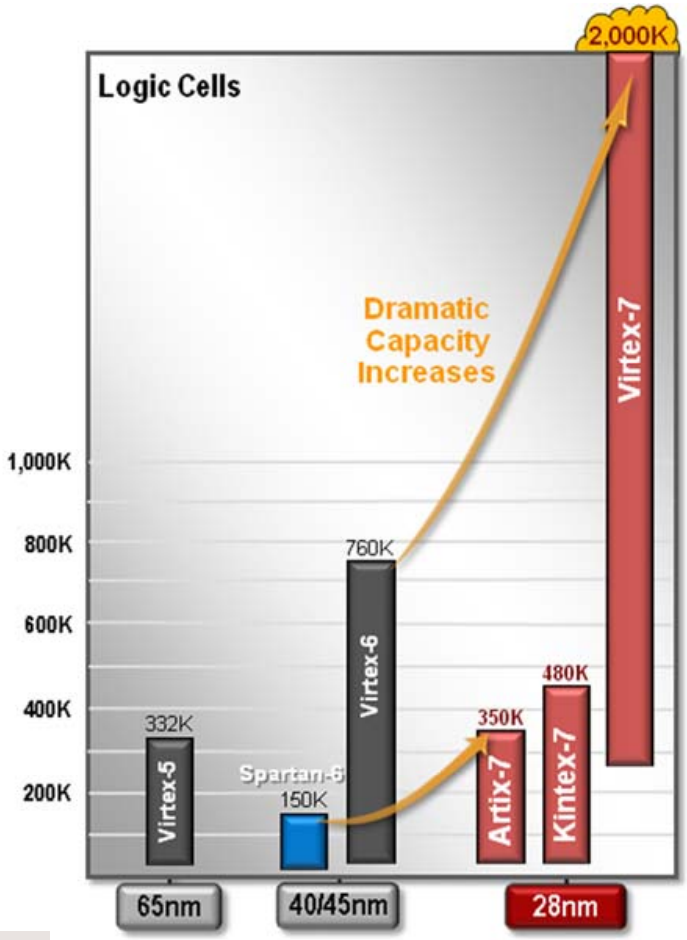
Exponential Growth in FPGA Capacity

Source: Xilinx

ASIC Prototyping … (2)

- Ever growing capacity can fit more logic in FPGA, therefore enabling entire SOC to be mapped on FPGA

- Challenges
  - Effective partitioning
  - Interconnect
  - Debug capabilities with growing logic complexity



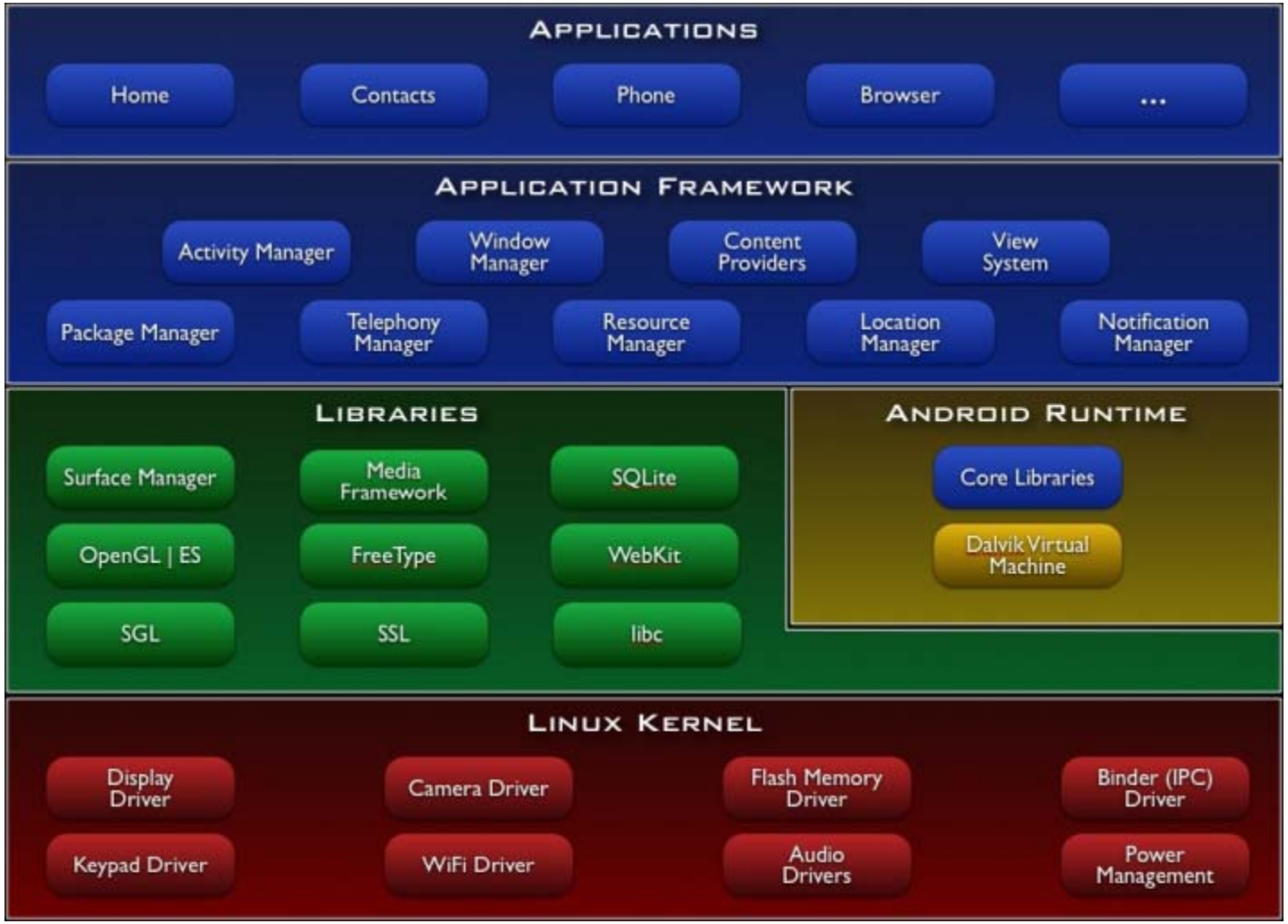
High ROI can be achieved when used ASIC prototyping efficiently

Source: Xilinx

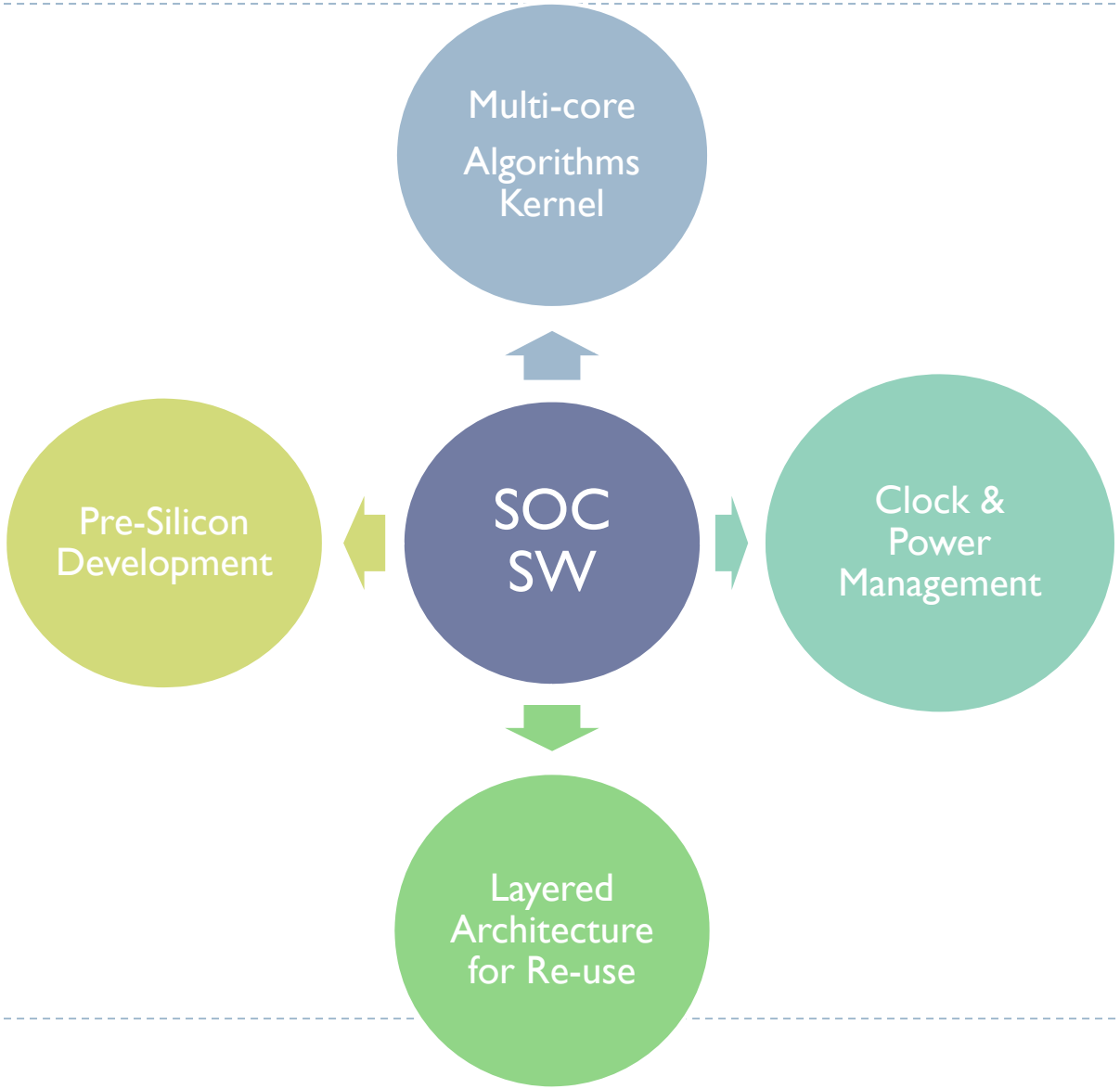
Low Power Design

- Design Tradeoffs
  - Standard Cell
  - Multi-Vt Design
- Clock Power
  - Major contributor to total active power (30-40%)
  - Separate Clock domains with independent PLLs
  - Clock Gating
  - Dynamic Frequency Scaling
- Multiple Power Domains
  - Dynamic Voltage Scaling
  - Voltage Islands with Power Gating
- Process Monitoring DVS

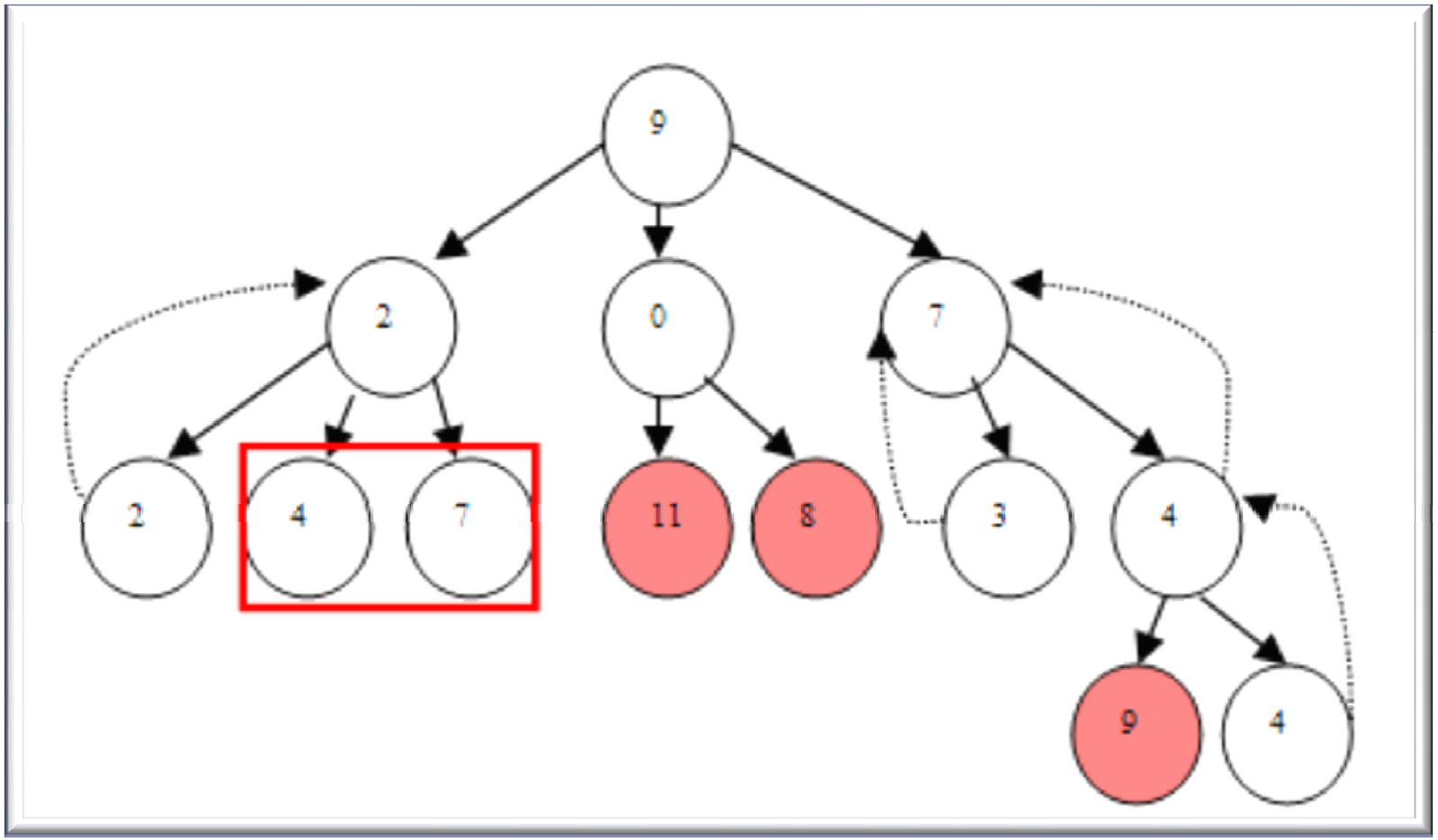
Android Architecture



Four Dimensions



Hierarchical Clock Tree Traversal



Manage branches of clock-tree for dynamic power management

Q& A