

LTE - Base Station Design Considerations and Challenges

Presenter -
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Technology-led Services Company

- TATA ELXSI - the Technology arm of the TATA group
- Headquartered in Bangalore
- Core Practice Areas- Embedded product design services, industrial design & engineering, Animation & Visual effects and System Integration Services
- Product Design Services focus on
 - Communications
 - Broadcast networks
 - Automotive
- International presence - US, Europe, APAC and Japan



World Class Systems & Processes

- Mature Quality Processes and Custom methodologies
- Assessed at SEI CMMI Level 5 and ISO 9001:2000
- Assessed at Auto SPICE Level 5
- Assessed at ISO 13485:2003 for Medical Product design
- BS 7799 certified Information Management Processes

Global Delivery Capabilities

- 3500+ team of designers, engineers & creative talent
- World-class Labs, Design Studios & Centers of Excellence



Communications Business Unit

VOIP, Unified Communications, Data Networking & Security Solutions, Next Gen Wireless Solutions



Broadcast Business Unit

Set top boxes, VOD & media servers, Media and authoring software, Multimedia codecs



MOTOROLA



Transportation Business Unit

Electronics for body, safety, power train and infotainment

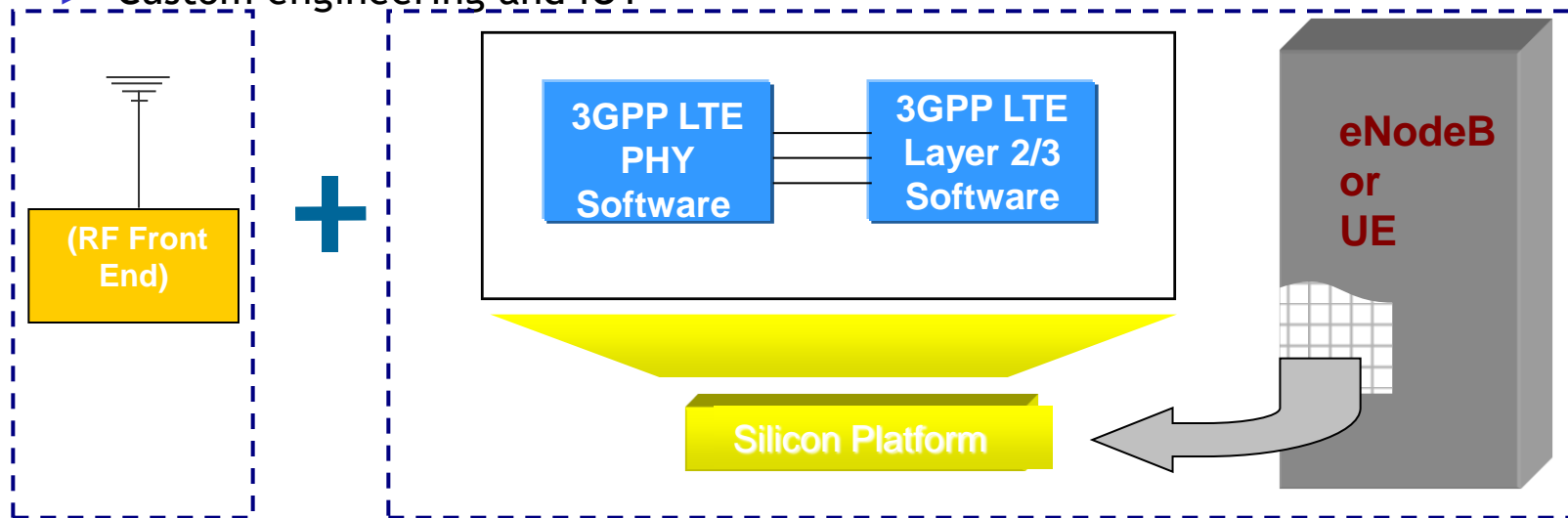


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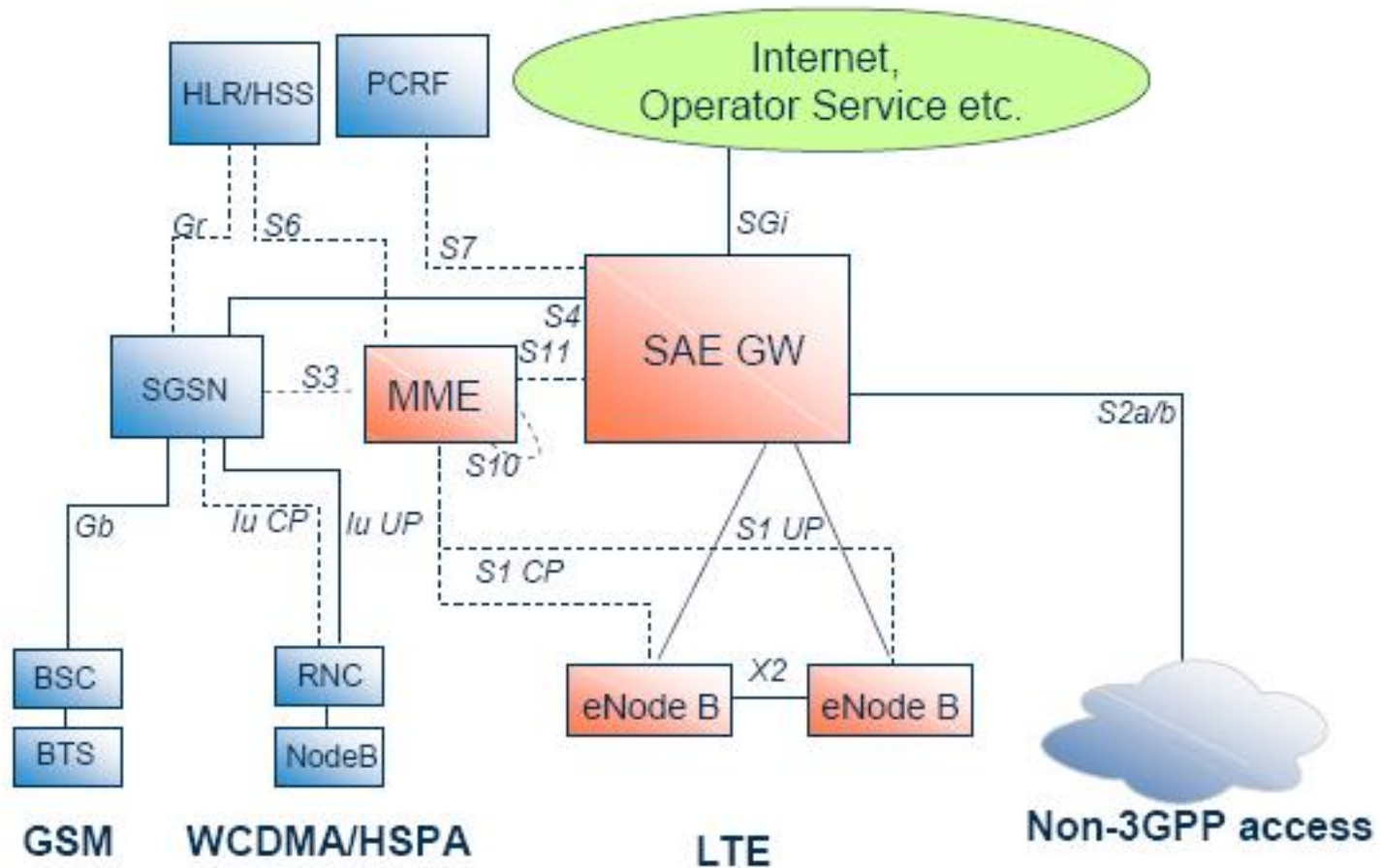


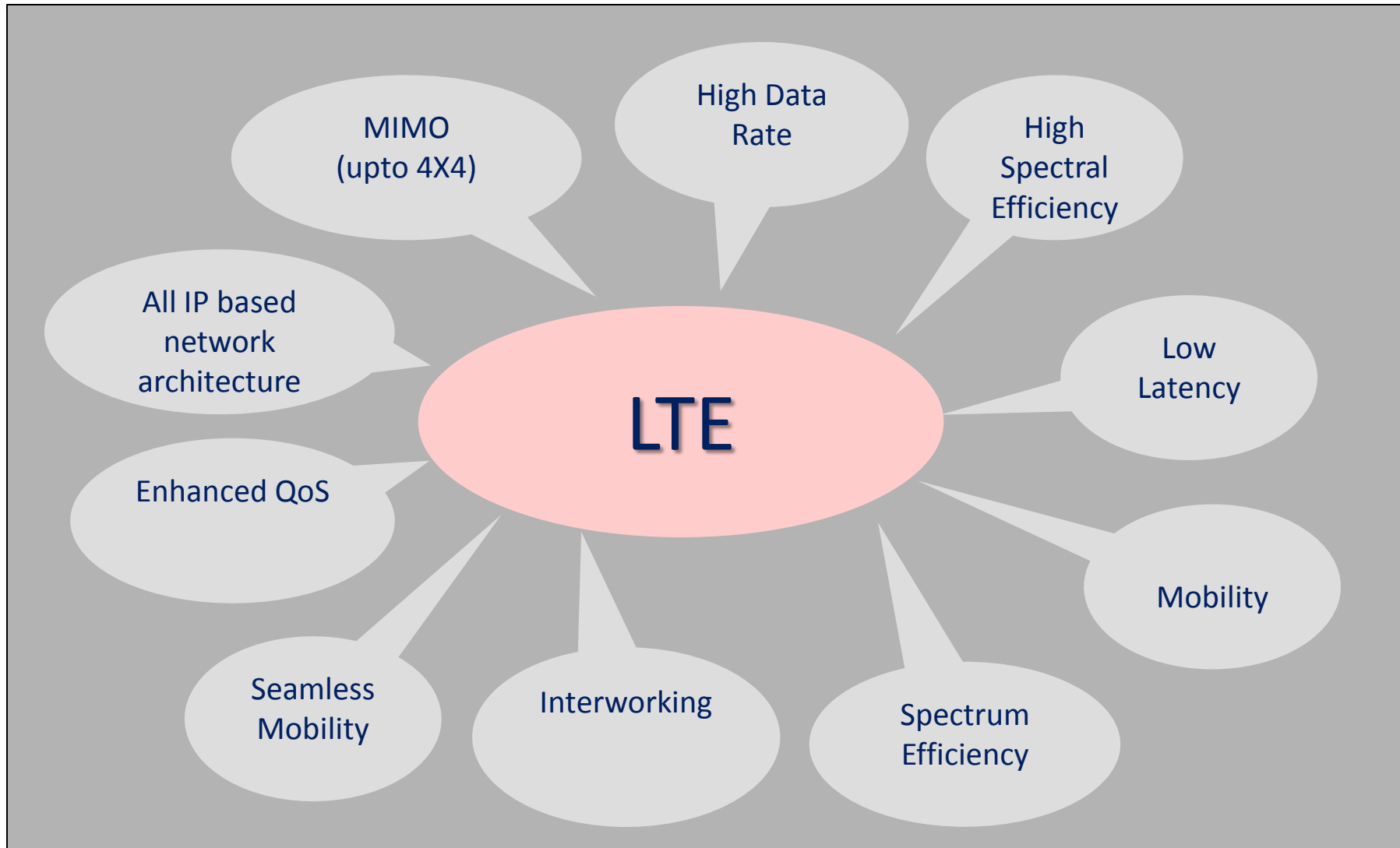
- ▶ **200+ engineering team**
 - ▶ 100 engineers dedicated to IP development
 - ▶ eNodeB Reference design integrated with Radio
 - ▶ UE emulator (complete UE L1 and L2/L3 protocol stack)
- ▶ **Product engineering Services for eNodeB and UE**
 - ▶ 100+ engineers engaged with leading customers
 - ▶ Custom engineering and IOT



-  Semiconductor platform
-  Tata Elxsi's LTE IPs
-  From RF Vendor Partner
-  OEM's LTE Product

LTE Network





- Latency
- High Throughput
- Spectral Efficiency
- 1 ms TTI
- QoS
- Carrier Aggregation
- Scalability of eNodeB to connect to multi MME and SGW

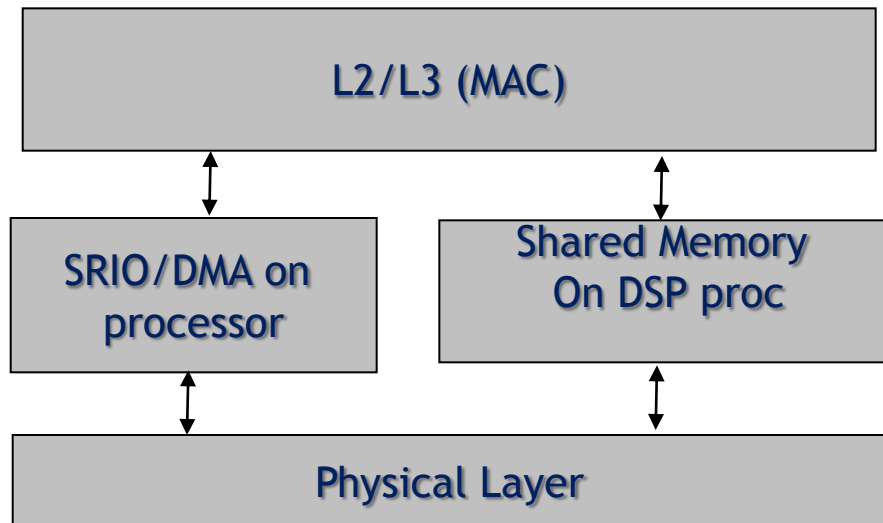
- Power Control and Inter-cell Interference Coordination (ICIC)
- *Coordinated multipoint (CoMP) transmission/reception*,
 - where transmission/reception is performed jointly across multiple cell sites (mainly) to improve cell-edge performance
- Multi Antenna Transmission
 - Diversity for improved system performance
 - Beam-forming for improved coverage (less cells to cover a given area)
 - Spatial-division multiple access (MU-MIMO) for improved capacity (more users per cell)
 - Multi-layer transmission (SU-MIMO) for higher data rates in a given bandwidth
- Backhaul design challenges

Platform specific

- Usage of multi core processors
 - Core partitioning -The key
 - High computational power
 - Optimum memory utilization
 - Usage of Data path accelerators
 - Usage of security engines
 - MPI interface (Gigabit Eth/SRIO/DMA/PCIXpress)
 - COTS platform for quick developments
 - Scalability
 - Portability to different platform
 - Time to market
 - Cost

- Time critical and computationally intensive jobs such as scheduler in a separate core
- Parallelism between the sub frame preparation for current sub frame and scheduler input meta-data preparation for next sub frame as different cores
- Computationally intensive job such as RoHC in separate cores
- Control plane functions in separate cores, grouped

MAC-PHY Interface Possible Abstraction (Logical View)



OS Specific :

- Control plane on Linux and User Plane on Light Weight Executive
- Control plane on Linux and User Plane on RTOS (eg. Enea/ VxWorks)
- Control plane and User plane on SMP Linux with RT patch and thread affinity

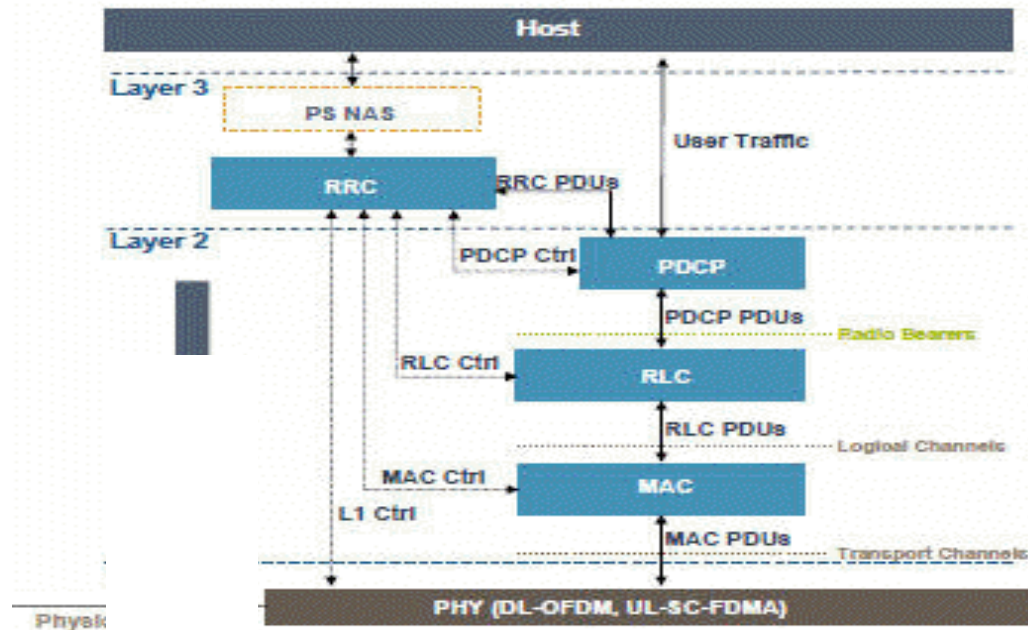
Software specific :

Task Partitioning And Prioritization

- Time critical jobs can be grouped under one task.
- Non time critical jobs can be grouped under a separate task
- Within the user plane, DL user plane and UL user plane can be grouped into separate tasks for effective DL transmissions
- Tasks handling time critical jobs assigned with higher priority
- User plane time critical jobs at higher priority than control plane tasks

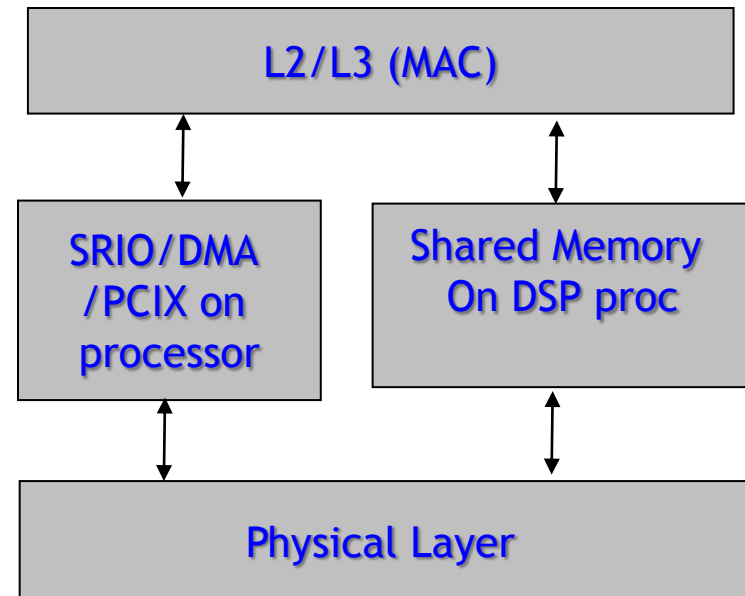
Data Plane Performance Considerations

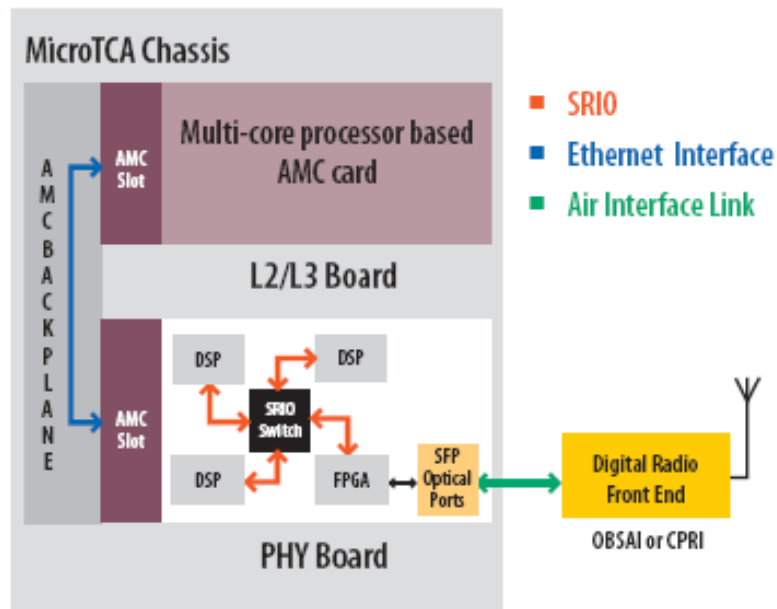
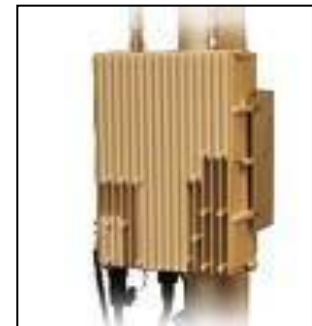
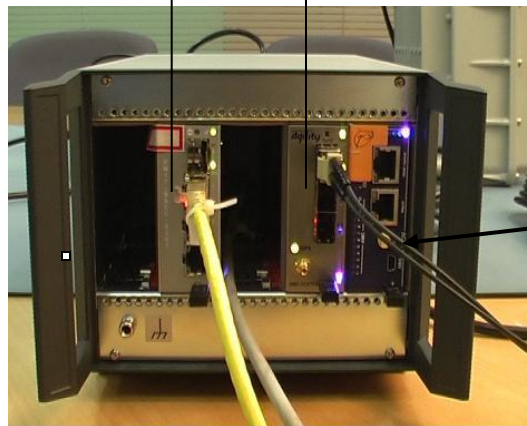
- Modules distribution and effective grouping
- Memory Pool Management
 - Deterministic Memory Allocation and De-allocation
- Buffer management
 - Zero Copy mechanism
 - Efficient Packet Processing w.r.t. Fragmentation, Concatenation, HARQ handling



- Usage of Memory Pool mechanism and Buffer Management
 - Services expected
 - Memory Allocation, De-allocation
 - Measurement of current memory utilization
 - Error indication on Pool Underflow
 - Error Indication on memory segment release in wrong Pool
 - Error indication on Double Free
 - Statistics

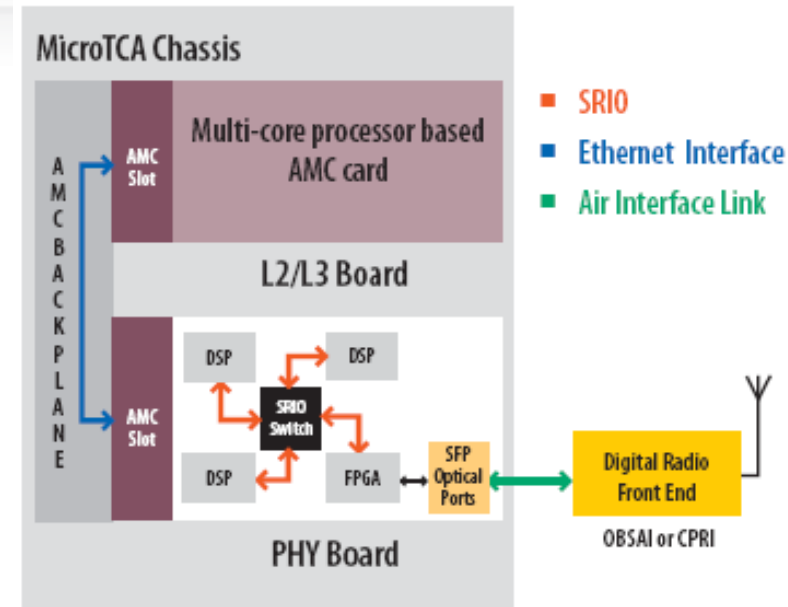
- MAC-PHY communication mechanism is independent on the physical link. It can be Gigabit Ethernet, SRIO, PCI express or any other communication interface
- MAC-PHY communication at every TTI
 - MAC - PHY communication considered to be error-free
 - PHY states are controlled by MPI
 - Need to supports Fragmentation and reassembly for normal/jumbo Ethernet
 - Maintains statistics information





▶ eNodeB Solution

- ▶ 3GPP Release 8 compliant
- ▶ 10 MHz; Scalable up to 20MHz
- ▶ 2x2 MIMO; Scalable up to 4x4
- ▶ FDD / TDD
- ▶ Integrated with RF
- ▶ Single / 3-sector solution



▶ Salient features

- ▶ Architectures for Femto/Pico, and Micro/Macro configurations
- ▶ Designed to support multi-core and multi-thread architecture to address scalability needs
- ▶ Femto/Pico architecture optimized for next-generation SOC architectures
- ▶ Well-defined interfaces for easy customization, or integration with 3rd party components
- ▶ Readily available for demonstration on COTS platform

Thank you



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